

KOPIO WBS Dictionary

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1.2.7

WBS Number	Descriptio
1.2.7	Trigger
1.2.7.1	Definition of the architecture Define the Trigger elements and their interconnection. Requires simulation work and a study of the requirements in connection with the F.E.E. development.
1.2.7.1.1	MC simulations
1.2.7.1.2	Analysis of F.E.E. performance
1.2.7.1.3	Specifications of trigger elements
1.2.7.1.4	Define interconnection protocols
1.2.7.2	Interconnection boards VME boards that implement the protocol of communication between different stages of the Trigger and include memories to feed the output and memories to read the inputs. These boards are developed as prototypes of the interconnection protocol.
1.2.7.2.2	Prototype development and test
1.2.7.2.3	Fabricate boards for test benches
1.2.7.3	Trigger digitizers: PR,CAL, veto 25MHZ ADC/TDC modules dedicated for the Trigger. They provide 10 bit pulse height information and 1ns time information for PM signals. Basic module is a 24 input module coming in two different flavors which differ for the digital signal processing.
1.2.7.3.1	TDC prototype development and test
1.2.7.3.2	ADC prototype development and test

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WBS Number	Descriptio
1.2.7.3.3	ASIC for analog preprocessing
1.2.7.3.4	Development of FPGA firmware for flavor A
1.2.7.3.5	Development of FPGA firmware for flavor B
1.2.7.3.6	Development and test of full board
1.2.7.3.7	Standalone bench test
1.2.7.3.8	Preproduction
1.2.7.3.9	ASIC production
1.2.7.3.10	Production
1.2.7.3.11	Installation and cabling
1.2.7.4	Module collector Each section of this board collects time/pulse height data from two serial inputs carrying data from 12 counters each, applies a programmable threshold to each signal and to their sum, producing suitable coded logical signals...
1.2.7.4.1	Design and review
1.2.7.4.2	Prototype development and test
1.2.7.4.3	Development and test of full board
1.2.7.4.4	Production
1.2.7.4.5	Installation and cabling
1.2.7.5	Strip routing cards These cards receive data from PR and calorimeter digitizers through a special crate backplane and rearrange them in groups of corresponding strips. Assuming that each module can handle 12 strips there would be 1 such module in a digitizer crate
1.2.7.5.1	Design and review

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WBS Number	Descriptio
1.2.7.5.2	Develop digitizer crate backplane
1.2.7.5.3	Routing card prototype development and test
1.2.7.5.4	Development and test of full board
1.2.7.5.5	Production
1.2.7.5.6	Fabricate and mount custom backplane
1.2.7.6	Strip collector This board perform sums of back to back strips in adjacent quadrants, applies thresholds to the individual "long" strips and performs sums in depth of the pulse height information of 9 modules. Each module receives input from 2 strip routing boards
1.2.7.6.1	Design and review
1.2.7.6.2	Prototype development and test
1.2.7.6.3	Development and test of full board
1.2.7.6.4	Production
1.2.7.6.5	Installation and cabling
1.2.7.7	Digitizers-collectors system test Set up a system including digitizers, strip transition boards, module collectors and strip collectors and exercise it with random pulses of variable rate. The system allows to read out each module separately in order to check the data
1.2.7.7.1	Set up hardware for test
1.2.7.7.2	Develop online software for test
1.2.7.7.3	Perform test and analyze data
1.2.7.8	Projection card Finds clusters in projection integrated in depth. Receives input from 2 strip collectors for each view. There is one board for the x view and one board for the y view.

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WBS Number	Descriptio
1.2.7.8.1	Design and review
1.2.7.8.2	Generation of test data
1.2.7.8.3	Prototype development and test
1.2.7.8.4	Construction
1.2.7.9	Pattern recognition card Receives digital signals from the strip collector of one view of the PR-CAL and applies pattern recognition algorithm
1.2.7.9.1	Design and review
1.2.7.9.2	Generation of test data
1.2.7.9.3	Prototype development and test
1.2.7.9.4	Construction
1.2.7.10	Boolean logic card Receives inputs in the form of zero suppressed time information on several channels and performs logic combination of them with time windows programmable for each input
1.2.7.10.1	Design and review
1.2.7.10.2	Generation of test data
1.2.7.10.3	Prototype development and test
1.2.7.10.4	Construction
1.2.7.11	Installation and cabling of the LV1 logic crate Connection of the logic cards in the detector area and installation of the cables between the detectors and the central logic. Cable centric logic.
1.2.7.12	Supervision and monitoring system

WBS	Descriptio
Number	
prescalable.	This system combines information from different sources to produce parallel Triggers individually selectable and It also distributes the Trigger information to the front end modules and handles busy signals from them.
1.2.7.12.1	System design
1.2.7.12.2	Alignment board development and test
1.2.7.12.3	Trigger formation board developmnet and test
1.2.7.12.4	Trigger transmitter development and test
1.2.7.12.5	Scalers
1.2.7.12.6	Fabrication
1.2.7.12.7	Installation and cabling
1.2.7.13	Clock system
information	Generation and distribution of a 25MHz clock synchronized to the extraction RF and capable of encoding Trigger and other control information.
1.2.7.13.1	Master clock
1.2.7.13.1.1	Design and review
1.2.7.13.1.2	Prototype and test
1.2.7.13.1.3	Fabricate and test
1.2.7.13.2	Clock drivers
1.2.7.13.2.1	Design and review
1.2.7.13.2.2	Prototype and test
1.2.7.13.2.3	Fabricate and test
1.2.7.13.3	Clock receivers
1.2.7.13.3.1	Design and review

WBS	Descriptio
Number	Descriptio
1.2.7.13.3.2	Prototype and test
1.2.7.13.3.3	Fabricate and test
1.2.7.13.4	Assemble, test, install system
1.2.7.14	Infrastructure
	This item includes hardware common to several subsystems, general services for the Trigger and tasks that can be grouped for budget and resource optimization
1.2.7.14.1	Crates
1.2.7.14.2	Crate interfaces (PCI?)
1.2.7.14.3	Cables
1.2.7.14.4	Readout controllers
1.2.7.14.5	Control CPU's
1.2.7.15	Commissioning
1.2.7.15.1	Develop trigger control programs
1.2.7.15.2	Develop trigger readout programs
1.2.7.15.3	Test logic chain with simulated data
1.2.7.15.4	Test logic chain + supervisor with simulated data
1.2.7.15.5	Test digitizers with cosmic rays or beam data
1.2.7.15.6	Test full chain
1.2.7.16	LV3 event selection software
1.2.7.17	Milestones and reviews
1.2.7.17.1	Finalize trigger options
1.2.7.17.2	Digitizers PDR

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WBS	
Number	Descriptio
1.2.7.17.3	Collector modules PDR
1.2.7.17.4	Logic modules PDR
1.2.7.17.5	Trigger supervisor PDR
1.2.7.17.6	Clock system PDR
1.2.7.17.7	Digitizers PRR
1.2.7.17.8	Collector modules PRR
1.2.7.17.9	Logic modules PRR
1.2.7.17.10	Trigger supervisor PRR
1.2.7.17.11	Clock system PRR